Claims

1. An electronic system, comprising:

a processor;

a memory having more than one memory location; and

a bus connecting the processor to the memory, wherein the bus comprises:

a data bus for transmitting data;

an address bus for identifying a first memory location;

a main command bus for transferring a first command that relates to the first memory location; and

a supplementary command bus for transferring a second command, wherein the second command does not relate to the first memory location.

2. An electronic system according to claim 1, wherein the second command is a PRECHARGE command, and wherein the supplementary command bus comprises a one-bit bus.

3. An electronic system according to claim 1, wherein:

the main command bus transfers location-specific commands; and

the supplementary command bus transfers only general commands.

4. An electronic system according to claim 1, wherein:

the second command is a secondary command indicator; and

the supplementary command bus transfers a third command after the second command.

5. An electronic system, comprising:

a processor;

a memory having more than one memory location; and

a bus connecting the processor to the memory, wherein the bus comprises:

a main command bus configured to transfer an address-specific command; and

a supplementary command bus configured to transfer a general command.

6. An electronic system according to claim 5, wherein the general command is a PRECHARGE command.

7. An electronic system according to claim 5, wherein:

the general command is a secondary command indicator; and

the supplementary command bus is further configured to transfer a third command after the second command.

8. A memory having an interface, wherein the interface comprises:

a location-specific command interface configured to receive location-specific commands; and

a general command interface configured to receive only one or more general commands.

9. A memory according to claim 8, wherein the general command interface is configured to receive a PRECHARGE command.

10. A memory according to claim 8, wherein the location-specific command interface is configured to receive location-specific commands and general commands.

11. A memory having an interface, wherein the interface comprises a general command interface configured to receive a general command.

12. A memory according to claim 11, wherein the general command is a PRECHARGE command.

13. A memory according to claim 11, wherein the memory includes more than one bank, and the interface further comprises a general bank select interface configured to receive bank address information for the general command.

14. A memory including a one-bit PRECHARGE input dedicated to receiving a PRECHARGE command.

15. A memory according to claim 14, wherein the memory includes more than one bank, further including a general bank select interface configured to receive bank address information for the PRECHARGE command.

16. A memory system, comprising:

a memory controller; and

a memory in communication with the memory controller, wherein the memory includes an interface, comprising:

a main control interface for receiving a location-specific command; and

a supplementary control interface for receiving a general command.

17. A memory system according to claim 16, wherein the general command is a PRECHARGE command.

18. A memory system according to claim 16, wherein:

the general command is a secondary command indicator; and

the supplementary control interface is configured to transfer a secondary command after the secondary command indicator.

19. An electronic system, comprising:

a processor; and

a memory system connected to the processor, comprising:

a memory controller connected to the processor; and

a memory connected to the memory controller and having an interface, comprising:

an address interface for receiving an address signal;

a main control interface, comprising:

a main command bus for receiving a first command signal relating to a memory location specified by the address signal; and

a main bank select bus for receiving a first bank select signal specifying a first bank corresponding to the first command signal; and

a supplementary control interface, comprising:

a supplementary command bus for receiving a second command signal, wherein the second command signal corresponds to a general command; and

a supplementary bank select bus for receiving a second bank signal specifying a second bank corresponding to the second command signal.

20. A method of accessing a memory, comprising:

in a first time slot, requesting activation of a first row;

in a second time slot, requesting an access of a memory location in the first row;

in a third time slot, requesting activation of a second row and requesting closure the first row.

21. A method according to claim 20, further comprising:

providing a main command bus, wherein the requesting activation of the second row occurs on the main command bus; and

providing a supplementary command bus, wherein the requesting closure of the first row occurs on the supplementary command bus.